AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A semiconductor memory, comprising:

a p-type semiconductor film provided on a p-type semiconductor substrate, a p-type well region in a semiconductor substrate, or an insulator;

a gate insulating film formed on the p-type semiconductor film provided on the p-type semiconductor substrate, the p-type well region in a semiconductor substrate, or the insulator;

a single gate electrode formed on the gate insulating film;

two charge storage sections formed on side walls of the gate electrode;

a channel region provided below the gate electrode; and

a first n-type diffusion layer region and a second n-type diffusion layer region provided to sides of the channel region,

wherein:

the charge storage sections are arranged to change an electric current flow between the first n-type diffusion layer region and the second n-type diffusion layer region under application of a voltage to the gate electrode according to a quantity of electric charge stored in the charge storage sections; and

the first n-type diffusion layer region is set to a reference voltage, the second n-type diffusion layer region is set to a voltage greater than the reference voltage, and the gate electrode is set to a voltage greater than the reference voltage, so as to inject electrons to one of the charge storage sections near the second n-type diffusion layer region.

2. (Previously Presented) The semiconductor memory of claim 1, wherein the p-type semiconductor film provided on the p-type semiconductor substrate, the p-type well region in the semiconductor substrate, or the insulator is set to a voltage less than the reference voltage.

3. (Original) The semiconductor memory of claim 1, wherein the first and second n-type diffusion layer regions have an offset structure where the gate electrode does not overlap the first and second n-type diffusion layer regions with the gate insulating film intervening therebetween.

4. (Original) The semiconductor memory of claim 1, wherein the charge storage sections overlap the channel region between the first n-type diffusion layer region and the second n-type diffusion layer region.

5. (Original) The semiconductor memory of claim 1, wherein:

the charge storage sections include a charge storing film capable of storing charge, a first insulating film, and a second insulating film; and

the charge storage sections have a structure where the charge storing film is sandwiched between the first insulating film and the second insulating film.

6. (Original) The semiconductor memory of claim 5, wherein:

the charge storing film is made of silicon nitride; and

the first and second insulating films are made of a silicon oxide.

7. (Original) The semiconductor memory of claim 5, wherein:

the first insulating film separates the charge storing film from the channel region or a well region; and

above the channel region, the first insulating film is at least 0.8 nm thick and is thinner than the gate insulating film.

8. (Original) The semiconductor memory of claim 5, wherein:

the first insulating film separates the charge storing film from the channel region or a well region; and

above the channel region, the first insulating film is at most 20 nm thick and is thicker than the gate insulating film.

9. (Original) The semiconductor memory of claim 5, wherein the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film.

10. (Original) The semiconductor memory of claim 5, wherein the charge storing film has a part extending substantially parallel to a side face of the gate electrode.

11. (Original) The semiconductor memory of claim 5, wherein the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film and also has a part extending substantially parallel to a side face of the gate electrode.

12. (Original) The semiconductor memory of claim 1, wherein the charge storage sections at least partly overlap part of the n-type diffusion layer regions.

13. (Original) The semiconductor memory of claim 1, further comprising p-type high concentration regions, adjacent to channel region sides of the n-type diffusion layer regions, which have a greater p-type impurity concentration than the channel region.

14. (Previously Presented) A semiconductor memory, comprising:

an n-type semiconductor film provided on an n-type semiconductor substrate, an n-type well region in a semiconductor substrate, or an insulator;

a gate insulating film formed on the n-type semiconductor film provided on the n-type semiconductor substrate, the n-type well region in the semiconductor substrate, or the insulator;

a single gate electrode formed on the gate insulating film;

two charge storage sections formed on side walls of the gate electrode;

a channel region provided below the gate electrode; and

a first p-type diffusion layer region and a second p-type diffusion layer region provided to sides of the channel region,

wherein:

the charge storage sections are arranged to change an electric current flow between the first p-type diffusion layer region and the second p-type diffusion layer region under application of a voltage to the gate electrode according to a quantity of electric charge stored in the charge storage sections; and

the first p-type diffusion layer region is set to a reference voltage, the second p-type diffusion layer region is set to a voltage less than the reference voltage, and the gate electrode is set to a voltage less than the reference voltage, so as to inject holes to one of the charge storage sections near the second p-type diffusion layer region.

15. (Previously Presented) The semiconductor memory of claim 14, wherein the n-type semiconductor film provided on the n-type semiconductor substrate, the n-type well region in the semiconductor substrate, or the insulator is set to a voltage greater than the reference voltage.

16. (Original) The semiconductor memory of claim 14, wherein the p-type diffusion layer regions have an offset structure where the gate electrode does not overlap the p-type diffusion layer regions with the gate insulating film intervening therebetween.

17. (Original) The semiconductor memory of claim 14, wherein the charge storage sections overlap the channel region between the first p-type diffusion layer region and the second p-type diffusion layer region.

18. (Original) The semiconductor memory of claim 14, wherein:

the charge storage sections include a charge storing film capable of storing charge, a first insulating film, and a second insulating film; and

the charge storage sections have a structure where the charge storing film is sandwiched between the first insulating film and the second insulating film.

19. (Original) The semiconductor memory of claim 18, wherein:

the charge storing film is made of silicon nitride; and

the first and second insulating films are made of a silicon oxide.

20. (Original) The semiconductor memory of claim 18, wherein:

the first insulating film separates the charge storing film from the channel region or a well region; and

above the channel region, the first insulating film is at least 0.8 nm thick and is thinner than the gate insulating film.

21. (Original) The semiconductor memory of claim 18, wherein:

the first insulating film separates the charge storing film from the channel region or a well region; and

above the channel region, the first insulating film is at most 20 nm thick and is thicker than the gate insulating film.

22. (Original) The semiconductor memory of claim 18, wherein the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film.

23. (Original) The semiconductor memory of claim 18, wherein the charge storing film has a part extending substantially parallel to a side face of the gate electrode.

24. (Original) The semiconductor memory of claim 18, wherein the charge storing film has a part having a surface substantially parallel to a surface of the gate insulating film and also has a part extending substantially parallel to a side face of the gate electrode.

25. (Original) The semiconductor memory of claim 14, wherein the charge storage sections at least partly overlap part of the p-type diffusion layer regions.

26. (Original) The semiconductor memory of claim 14, further comprising n-type high concentration regions, adjacent to channel region sides of the p-type diffusion layer regions, which have a greater n-type impurity concentration than the channel region.

27. (Previously Presented) The semiconductor memory of claim 5, wherein:

the charge storing film includes a first part and a second part, the first part having a surface substantially parallel to a surface of the gate insulating film, the second part extending substantially parallel to a side face of the gate electrode; and

the first n-type diffusion layer region and the second n-type diffusion layer region are formed so that the channel region faces an end of the second part in a thickness direction of the gate electrode.

28. (Previously Presented) The semiconductor memory of claim 27, wherein:

the first part extends outward from an end of the second part in the thickness direction of the gate electrode, the end facing the channel region.

29. (Previously Presented) The semiconductor memory of claim 28, wherein:

the first part partly overlaps either the first n-type diffusion layer region or the second n-type diffusion layer region.

30. (Previously Presented) The semiconductor memory of claim 18, wherein:

the charge storing film includes a first part and a second part, the first part having a surface substantially parallel to a surface of the gate insulating film, the second part extending substantially parallel to a side face of the gate electrode; and

the first p-type diffusion layer region and the second p-type diffusion layer region are formed so that the channel region faces an end of the second part in a thickness direction of the gate electrode.

31. (Previously Presented) The semiconductor memory of claim 30, wherein:

the first part extends outward from an end of the second part in the thickness direction of the gate electrode, the end facing the channel region.

32. (Previously Presented) The semiconductor memory of claim 31, wherein:

the first part partly overlaps either the first p-type diffusion layer region or the second p-type diffusion layer region.

33. (Previously Presented) The semiconductor memory of claim 4, wherein:

the overlap W2-W1 of the charge storage sections and the channel region is greater than 10 nm, where W1 is the amount of offset between edge of the gate electrode and either of the first and second diffusion layer regions, W2 is the width of the charge storage section taken along the channel length of the channel region.

34. (Previously Presented) The semiconductor memory of claim 14, wherein:

the overlap W2-W1 of the charge storage sections and the channel region is greater than 10 nm, where W1 is the amount of offset between edge of the gate electrode and either of the first and second diffusion layer regions, W2 is the width of the charge storage section taken along the channel length of the channel region.

35. (New) The semiconductor memory of claim 1, wherein

the first n-type diffusion layer region is set to the reference voltage, the second n-type diffusion layer region is set to a voltage greater than the reference voltage, the gate electrode is set to a voltage greater than the reference voltage and less than the voltage of the second n-type diffusion layer region, so as to inject electrons to one of the charge storage sections near the second n-type diffusion layer region.

36. (New) The semiconductor memory of claim 14, wherein

the first p-type diffusion layer region is set to the reference voltage, the second p-type diffusion layer region is set to a voltage less than the reference voltage, the gate electrode is set to a voltage less than the reference voltage and greater than the voltage of the second p-type diffusion layer region, so as to inject holes to one of the charge storage sections near the second p-type diffusion layer region.

37. (New) The semiconductor memory of claim 6, wherein:

the silicon nitride film has a thickness of 2 nm to 15 nm; and

if the first insulating film and the second insulating film are made of a silicon oxide, the silicon oxide films each have a thickness of 1.5 nm to 10 nm.

38. (New) The semiconductor memory of claim 19, wherein:

the silicon nitride film has a thickness of 2 nm to 15 nm; and

if the first insulating film and the second insulating film are made of a silicon oxide, the silicon oxide films each have a thickness of 1.5 nm to 10 nm.

39. (New) The semiconductor memory of claim 1, wherein

the gate electrode does not cover the charge storage sections.

40. (New) The semiconductor memory of claim 14, wherein

the gate electrode does not cover the charge storage sections.